

CLAIMS

1. An interface circuit alternately configurable in one of a first communication protocol mode for communicating in a first communication protocol and a second communication protocol mode for communicating in a second communication protocol, and for interfacing an associated device with an external device for communicating the associated device with the external device in one of the first communication protocol and the second communication protocol, the interface circuit being configured in the first protocol mode on power-up, the interface circuit comprising
 - a plurality of communication terminals for communicating signals in the first and second protocols between the interface circuit and the external device, the number of communication terminals required not exceeding the number of communication terminals required to communicate in the one of the first and second protocols which requires the greatest number of communication terminals, and
 - a monitoring circuit for monitoring one of the communication terminals for a protocol select signal, and being responsive to the protocol select signal for configuring the interface circuit in the second protocol mode.
2. An interface circuit as claimed in Claim 1 in which a locking circuit responsive to the monitoring circuit detecting the protocol select signal is provided for locking the interface circuit configured in the second protocol mode.
3. An interface circuit as claimed in Claim 2 in which the locking circuit is responsive to the monitoring circuit detecting the protocol select signal for locking the interface circuit configured in the first protocol mode.
4. An interface circuit as claimed in Claim 2 in which the locking circuit releasably locks the interface circuit in the configured protocol mode.
5. An interface circuit as claimed in Claim 2 in which the locking circuit is responsive to powering down of the interface circuit for releasing the interface circuit from the configured protocol mode.

6. An interface circuit as claimed in Claim 1 in which a signal processing circuit is provided, the signal processing circuit being selectively and alternately configurable in one of the first and second protocol modes for processing the communication signals in the respective first and second protocols, the signal processing circuit being configurable in the 5 respective first and second protocol modes in response to first and second mode select signals, respectively.

7. An interface circuit as claimed in Claim 6 in which a switch circuit is provided, the switch circuit being selectively and alternately operable in one of a first state and a second 10 state in response to the monitoring circuit, the switch circuit being operable in the first state in response to the monitoring circuit on power-up of the interface circuit for applying the first mode select signal to the signal processing circuit.

8. An interface circuit as claimed in Claim 7 in which the switch circuit is operable in 15 the second state in response to the monitoring circuit detecting the protocol select signal for applying the second mode select signal to the signal processing circuit.

9. An interface circuit as claimed in Claim 7 in which the switch circuit is operable in the second state in response to the monitoring circuit detecting the protocol select signal for 20 applying the first mode select signal to the signal processing circuit.

10. An interface circuit as claimed in Claim 7 in which the switch circuit is operable in the first state in response to one of a high and low logic state of a switch signal outputted by the monitoring circuit, and the switch circuit is operable in the second state in response to the 25 other of the high and low logic states of the switch signal outputted by the monitoring circuit.

11. An interface circuit as claimed in Claim 7 in which the first mode select signal is one of a logic high and a logic low signal, and the second mode select signal is the other of a logic high or a logic low signal.

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12. An interface circuit as claimed in Claim 11 in which the logic high signal which provides the one of the first and second mode select signals is provided by the supply voltage

of the interface circuit, and is applied to the signal processing circuit through the switch circuit when the switch circuit is in the first state.

13. An interface circuit as claimed in Claim 11 in which the logic low signal which
5 provides the one of the first and second mode select signals is provided by ground of the interface circuit, and is applied to the signal processing circuit through the switch circuit when the switch circuit is in the second state.

14. An interface circuit as claimed in Claim 7 in which one of the communication
10 terminals is adapted for selectively receiving one of the first and second mode select signals simultaneously with the protocol select signal being applied to another one of the communication terminals, and a mode signal latching means is provided responsive to the protocol select signal for latching the one of the first and second mode select signals applied to the communication terminal.

15. An interface circuit as claimed in Claim 15 in which the latched one of the first and second mode select signals is applied from the mode signal latching means to the signal processing circuit through the switch circuit, when the switch circuit is in the second state.

20 16. An interface circuit as claimed in Claim 7 in which the switch circuit comprises a multiplexer.

17. An interface circuit as claimed in Claim 10 in which the monitoring circuit comprises a first state machine for monitoring the communication terminal on which the protocol select
25 signal is to be applied, and for outputting one of a logic high and a logic low signals in response to the interface circuit being powered up, and the other of the logic high and the logic low signals on the protocol select signal being detected, the switch signal outputted by the monitoring circuit being derived from the logic signal outputted by the first state machine.

30 18. An interface circuit as claimed in Claim 17 in which a switch signal latching means is provided for alternately latching the switch signal in the one of the high and low logic states in response to the logic state of the output signal of the first state machine.

19. An interface circuit as claimed in Claim 18 in which the switch signal latching means is responsive to the protocol select signal after power-up of the interface circuit for altering the logic state of the switch signal for operating the switch circuit from the first state to the 5 second state, and for latching the switch signal in the altered logic state.

20. An interface circuit as claimed in Claim 19 in which the locking circuit comprises an inverter for inverting the switch signal, and an AND gate for ANDing the inverted switch signal with the output signal of the first state machine and for applying the ANDed signal to 10 the switch signal latching means, the switch signal latching means being responsive to the output of the AND gate for altering the logic state of the switch signal for operating the switch circuit in the second state in response to the protocol select signal after power-up, and the AND gate is responsive to the altered logic state of the switch signal for inhibiting the protocol select signal being applied to the switch signal latching means, so that the switch 15 signal latching means retains the switch signal latched in the altered logic state.

21. An interface circuit as claimed in Claim 6 in which a second state machine is provided, the second state machine being responsive to the mode select signal applied to the signal processing circuit for applying a timing select signal to the signal processing circuit, 20 for selecting the timing of the signal processing circuit to correspond with the one of the first and second protocol modes in which the signal processing circuit is configured.

22. An interface circuit as claimed in Claim 1 in which the protocol select signal comprises a signal which transitions from one of high and low states to the other of the high 25 and low states.

23. An interface circuit as claimed in Claim 22 in which the monitoring circuit is responsive to one of a rising and falling edge of the protocol select signal as the protocol select signal transitions from the one of the high and low states to the other of the high and 30 low states.

24. An interface circuit as claimed in Claim 22 in which the monitoring circuit is responsive to a predetermined number of edges of the protocol select signal as the protocol select signal transitions from the one of the high and low states to the other of the high and 5 low states.

25. An interface circuit as claimed in Claim 24 in which the monitoring circuit is responsive to a predetermined number of rising edges of the protocol select signal.

10 26. An interface circuit as claimed in Claim 1 in which one of the first and second protocols is SPI protocol, and the other of the first and second protocols is one or both of I²C and SMBus protocols.

15 27. An interface circuit as claimed in Claim 26 in which at least three communication terminals are provided for facilitating communication in both the SPI protocol and one or both of the I²C and SMBus protocols.

20 28. An interface circuit as claimed in Claim 27 in which one of the communication terminals is a clock signal receiving terminal for receiving clock signals for communicating in the SPI protocol and one or both of the I²C and SMBus protocols, and one of the communication terminals is a chip enable terminal for receiving a chip enable signal for communicating in the SPI protocol.

25 29. An interface circuit as claimed in Claim 26 in which at least one of the communication terminals is a serial data address terminal for communicating serial data in the SPI protocol, and for communicating serial data and addresses in one or both of the I²C and SMBus protocols.

30 30. An interface circuit as claimed in Claim 29 in which two of the communication terminals are serial data address terminals, one of which communicates serial data into the interface circuit, and one of which communicates serial data out of the interface circuit in the SPI protocol, and one of the two serial data address terminals communicates serial data and

addresses with the interface circuit in one or both of the I²C and SMBus protocols.

31. An interface circuit as claimed in Claim 30 in which terminal is provided for receiving clock signals for communicating in the I²C and/or SMBus protocols, and one of the
5 two serial data address terminals communicates addresses with the interface circuit in one or both of the I²C and SMBus protocols.

32. An interface circuit as claimed in Claim 26 in which the first protocol is one or both of the I²C and SMBus protocols.

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33. An interface circuit as claimed in Claim 28 in which the chip enable terminal is adapted for receiving the protocol select signal.

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34. An interface circuit as claimed in Claim 29 in which one of the serial data address terminals is adapted for receiving the first and second mode select signals.

35. An integrated circuit comprising an interface circuit as claimed in Claim 1, and an associated device, the interface circuit being provided for communicating the associated device with an external device in either of the first protocol and the second protocol.

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36. An integrated circuit comprising:

an interface circuit, and

an associated device, wherein

the interface circuit is alternately configurable in one of a first communication

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protocol mode for communicating in a first communication protocol and a second communication protocol mode for communicating in a second communication protocol, and for interfacing the associated device with an external device for communicating the associated device with the external device in one of the first communication protocol and the second communication protocol, the interface circuit being configured in the first protocol
30 mode on power-up, the interface circuit comprising

a plurality of communication terminals for communicating signals in the first and second protocols between the interface circuit and the external device, the number of communication terminals required not exceeding the number of communication terminals required to communicate in the one of the first and second protocols which requires the greatest number of communication terminals, and

5 a monitoring circuit for monitoring one of the communication terminals for a protocol select signal, and being responsive to the protocol select signal for configuring the interface circuit in the second protocol mode.

10 37. A method for communicating through an interface circuit between a device associated with the interface circuit and an external device in either one of a first communication protocol and a second communication protocol, the method comprising the steps of:

15 providing the interface circuit with a plurality of communication terminals for communicating with the external device, the number of communicating terminals required not exceeding the number of communicating terminals required to communicate in the one of the first and second protocols which requires the greatest number of communication terminals,

20 providing the interface circuit with a monitoring circuit for monitoring one of the communication terminals for a protocol select signal,

25 configuring the interface circuit in a first protocol mode on power-up of the interface circuit for communicating in the first protocol,

monitoring the one of the communication terminals by the monitoring circuit for the protocol select signal, and

configuring the interface circuit in a second protocol mode for communicating in the second protocol in response to detection of the protocol select signal.

38. A method as claimed in Claim 37 in which the interface circuit is locked configured in the second protocol mode in response to the protocol select signal.

30 39. A method as claimed in Claim 38 in which the interface circuit is locked configured in the first protocol mode in response to the protocol select signal.

40. A method as claimed in Claim 38 in which the interface circuit is releasably locked in the configured protocol mode.

41. A method as claimed in Claim 38 in which the interface circuit is released from the
5 configured protocol mode in response to powering-down of the interface circuit.